# Modeling of Voltage Control Oscillator based Delta-Sigma ADC

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**ABSTRACT**

This paper presents a third-order Voltage Control Oscillator (VCO) based Delta-Sigma ADC with two integrators. The modulator topology is cascade of integrator with multiple feedback. The design consists of two integrators and VCO based quantizer is used. Due to VCO based design the second-order modulator gives a third-order noise shaping. A 5-stages VCO based quantizer is used which gives 2-bit quantization. The coefficients for integrator are calculated from the MATLAB by keeping the design optimization and oversampling ratio (OSR) of 25. A sampling frequency of this modulator is 950 MHz while the input frequency is 2.43 MHz. The modulator design for the signal bandwidth of 19 MHz with an oversampling ratio of 25. The third-order modulator can achieve signal-to-noise ratio (SNR) of 85dB and signal-to-noise-plus-distortion (SNDR) of 77.4dB.

**Keywords**: Signal transfer function, DC gain, Noise transfer function, Operational amplifier

## 1. INTRODUCTION:

Today demand of low power analog to digital converters for different communication devices. During the recent publications it shows that a voltage control oscillator-based Delta-Sigma Analog to digital converters has many advantages. Most of the part of VCO based ADC is digital so it provides fast communication. Another advantage of VCO based ADC is that a voltage control oscillator work as a quantizer and integrator also so it reduces the complexity of circuits. A second-order multi-bit delta-sigma modulator is modeled and simulated for hearing signals. The modulator can achieve 16-bit resolution with an oversampling ratio of 128. The complete modulator circuit non-idealities like limited DC gain, limited slew-rate, thermal noise, and flicker noise, modeled and simulated. A voltage control oscillator-based integrator and quantizer use in a continuous time delta sigma analog to digital converter is presented in this paper [1]. The bandwidth of the signal is 20MHz and it achieve a high resolution. This circuit is implemented in 0.13um CMOS process technology. It achieves a SNDR of 78.1dB while the signal to noise ratio of 81.2dB. The power consumption of this overall circuit is 87mW while the supply voltage is of 1.5V. To avoid signal distortion, it uses the oscillator's phase output which remove the limitations of performance which is being faced in all those earlier publications that uses its frequency output only. The presented

model provides 4th order noise shaping by using only 3 operational amplifier-based integrators. This [2] paper present a 2nd order continuous time delta sigma modulator using VCO based design. In this design VCO is used at 2nd stage. Noise shaping order is increased by using residue cancelling quantizer. The modulator is design in 90nm CMOS technology and occupied 0.36mm$^2$ area. The power consumption of analog to digital converter is 16mW.The sampling frequency of this modulator is 600MHz while the signal bandwidth is of 10MHz. It achieves an SNDR of 78.3dB while SFDR is of 85dB.There are many advantages of voltage control oscillator-based design which is suitable for analog to digital converter which include the 1st order noise shaping, power efficiency and implicit dynamic element matching. By taking advantage of these a two step VCO based ADC is designed and implemented in this paper [3]. As the input has intrinsic DEM the DAC matching is relaxed. By using simple open loop structure and more digital part a high bandwidth and stable performance easily be achieved. The modulator achieves a 59.5dB SNDR while the SFDR is of 67.6dB with signal bandwidth of 40MHz. The sampling frequency for this modulator is 1.6GHz while the power consumption is only 2.7mW. In another paper [4] the modeling as well as design is presented for time-based analog to digital converter architecture in which VCO is used and high linearity is achieved. In this design voltage control oscillator is operate through a time domain PWM signal instead of driving a VCO by a continuous time analog signal. Operating point of VCO is defined by discrete levels of PWM waveform only. A high performance ADSM drive the VCO which convert continuous analog input amplitude to self-oscillating PWM pulse. To guarantee the linearity only two points on $K_{vco}$ nonlinear transfer curve are selected. Another addition is that the quantization error of phase between two consecutive samples is generated by phase detector and then it is processed by VCO at 2nd stage. By combining the output of the 1st VCO a time domain VCO based MASH 2Nd order noise shaping delta sigma ADC is obtained. All the process is fabricated in 90nm CMOS technology. Without any calibration it obtains a SFDR more than 67dB with bandwidth of 20MHz. Analog and mixed signal-based circuits design techniques relaying maximum on the use of Operational amplifier so that it can process signals into voltage domain. But it faces many difficulties in advanced CMOS process. To overcome these issues in this paper [5] a synthesis friendly scaling compatible ring VCO based time domain delta sigma ADC is presented. By using this the performance improves as technology advances. Its maximum part includes digital design. Decompose into digital logic gates and resistors a small set of customized cells its layout becomes fully synthesizable by leveraging digital layout synthesis tools. Post layout simulations are also performed. It will explain the scaling compatibility of ADC and drastic boost to design productivity. In another paper [6] A voltage control oscillator based continuous time delta sigma ADC is designed. In this design a new feedforward VCO scheme is proposed which is contributing to higher oscillation frequency. In this design a 4th order noise shaping of Delta sigma ADC is obtained by using only three operational transconductance amplifiers. At 4th stage a VCO is attached which work as an integrator as well as quantizer. Along with this an excess loop delay is also introduced by finite gain bandwidth product which is compensated by zero order path in loop filter which reduce

power consumption. After performing simulations this design achieves SNDR of 72.17dB while the bandwidth is of 10MHz. the sampling frequency is 400MHz.The ADC work with supply voltage of 1.8V while the power consumption is of 24mW. All the simulations Is performed in 180nm CMOS technology. This paper present [7] present a quantization noise filtering techniques for a wideband delta sigma fractional-N phase locked loop. By two step phase interpolation a single path finite impulse response filtering techniques is realized. The sampling frequency for this fractional-N PLL is 1.6GHz with bandwidth of 1.5MHz wide loop bandwidth is designed in 130nm CMOS technology. After simulations results shows that this method reduces the high frequency quantization noise by 12dB and attain in band phase noise of -101dBc/Hz at 400kHz and 2.14ps integrated jitter. The power consumption of this topology is 3.3mW and is covers an area of 0.24mm$^2$

## 2. MATERIALS AND METHODS

A voltage control oscillator based quantizer consists of a set of registers which is a DFF, an XOR gates and then finally adder is implemented. As this circuit becomes simple so it attains a high-speed operation with less latency, an important characteristic of VCO. In this structure a VCO delay cells gives output which is given to input of the DFF. Another pair of DFF is attached after this which take the output of previous DFF and convert it into output. Both DFFs output are then given to the input of the XOR gates and then finally adder add them. The modelling process is done using Delta sigma Toolbox which easily available on google and then cppsim view software. By using this toolbox, we start modelling. Assume that there is no excess loop delay the DT loop filter is designed by using sigma delta toolbox, and then results is taken from the MATLAB. Here we must select the sampling frequency of the modulator, the oversampling ratio of the modulator and analog bandwidth. The sampling frequency is selected 950MHz while the oversampling ratio is of 25. The result is presented in figure1 which is without excess loop delay. A 2$^{nd}$ order continuous time loop filter must take into consideration of excess loop delay. Here we chose a clock delay of simply 1 clock period without any significant error. For the compensation of this delay a minor compensation loop is included at quantizer. Here the NTF is still same as previous, but the STF is modified. The results are shown in the figure 2nd. Now we must convert DT loop filter to a continuous time loop filter and plot the results by using same toolbox in MATLAB. Plot of magnitude and phase response of open loop gain which is shown in figure3.

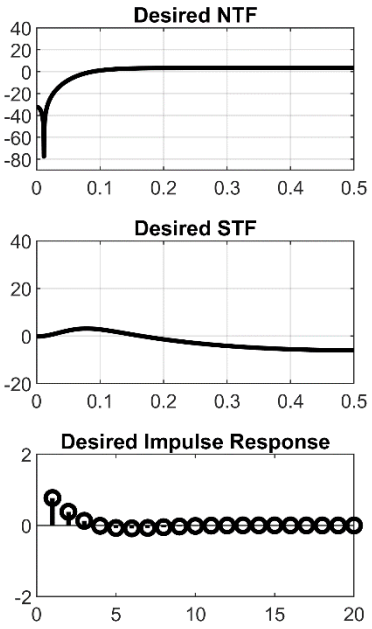


**Figure 1**

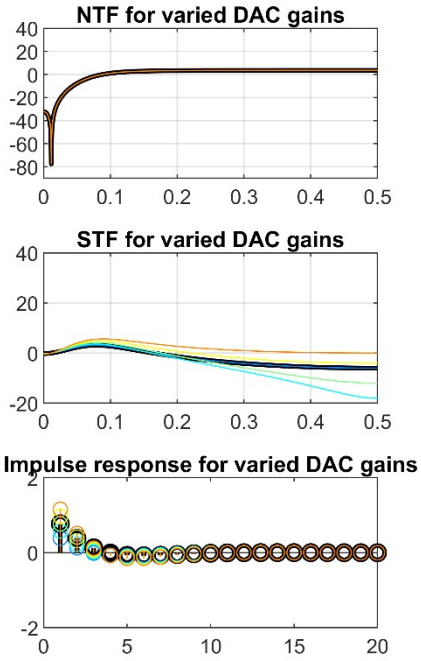


**Figure 2**

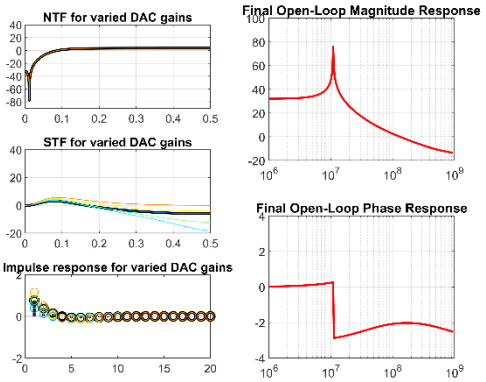


**Figure3**

As open loop continuous time transfer function established, now we have to calculate the parameters for loop filter by assuming the $K_v$, DAC gains etc. After calculating this with NTF zero optimization and the bandwidth is of 20MHz we now process 2nd order loop filter in Cppsim view. Put all the values into the ADC select VCO 5 stages we calculate the performance parameters by using MATLAB and Cppsim view. All the part includes in Cppsim view which consist of two integrators and Voltage control oscillator. The output of the integrator is shown in the figure 4.

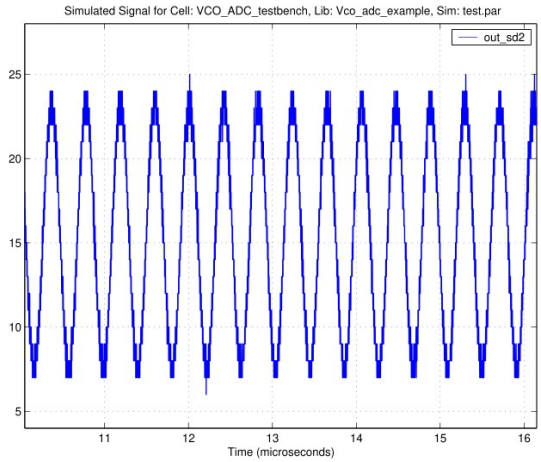


**Figure 4**

After getting the output of the integrator from the Sue2 now we go to MATLAB and

type command in command section post.m which will produce the PSD plot of the modulator which is shown in the figure 5. From this plot we can see that 2nd order continuous time delta sigma ADC provide a 3rd order noise shaping.

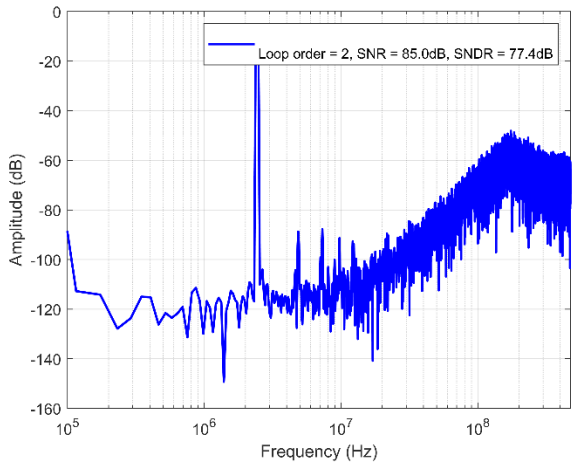


**Figure 5**

Here we can see that the modulator attains a 3rd order noise shaping by using only two integrators and a VCO based quantizer. The Signal to noise ratio is obtained from this is 85dB while the SNDR is of 77.4dB.

## 3. CONCLUSION

A modelling of 3rd order continuous time Voltage control oscillator-based delta sigma analog to digital converter is presented in this paper for hearing aid. The topology of the modulator is CIFB to lower the power of the loop filter. Here we can see that the NTF and STF plot is obtained with and without excess loop delay. After this a DT to CT conversion is performed using a Sigma delta toolbox of MATLAB. Then by assuming some values coefficients are calculated. After this these coefficients are put into parameters values and then simulation is performed on Cppsim view which gives us the output of the integrator. The final Output PSD plot is obtained from MATLAB using post.m function. This will also provide the performance parameters like SNR is of 85dB with SNDR is of 77.4dB.

## 4. REFERENCES

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